Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : New assembly and test line qualification for Rectifiers STTHxxDJF-TR and STPSxxDJF-TR housed in PowerFLATTM 5x6 package

PCN Reference : ADG/22/13659

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STTH8R03DJF-TR	STTH5R06DJF-TR	STPS15L30CDJFTR
STTH30R02DJF-TR	STPS30H100DJF-TR	STPS30M60DJF-TR
STPS30L30DJF-TR		

IMPORTANT NOTICE – PLEASE READ CAREFULLY

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Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

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Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

PCN
Product/Process Change Notification

New assembly and test line qualification for Rectifiers STTHxxDJF-TR and STPSxxDJF-TR housed in PowerFLAT™ 5x6 package

Notification number:	ADG/22/13659	**Issue Date**	20-Sept-2022
Issued by	Sophie da Silva		
Product series affected by the change		STTH30R02DJF-TR STTH5R06DJF-TR STTH8R03DJF-TR STPS15L30CDJFTR STPS30H100DJF-TR STPS30L30DJF-TR STPS30M60DJF-TR	
Type of change		Back-End realization	

Description of the change

Qualification of a back-end subcontractor located in China (location B) for the assembly and test and finishing of Rectifiers products in PowerFLAT™ 5x6.
The production currently located ST Shenzhen in China (location A) will be extended with subcontractor in China (location B) for Rectifiers products in PowerFLAT™ 5x6.
This subcontractor in China (Location B) is already a major production site for ST products (FERD, Power Schottky and Ultrafast diodes technologies), including PowerFLAT™ 5x6 package (with slight difference of package drawing compared to location A).

Reason for change

STMicroelectronics investment on Rectifiers production capacity increase.

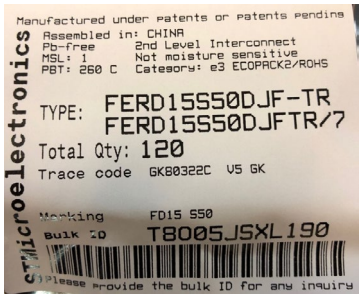
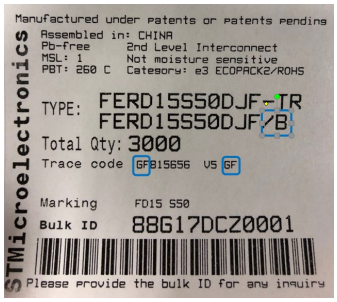
Former versus changed product:	The changed products do not present modified electrical or thermal parameters. New recommended footprint (both locations compatible). Refer to next page. The Moisture Sensitivity Level of the part (according to the IPC/JEDEC JSTD-020D standard) remains unchanged. There is no change in the packing modes and the standard delivery quantities either. The products remain in full compliance with the ST ECOPACK®2 grade (so called “halogen-free”).

(1) ADG: Automotive and Discrete Group

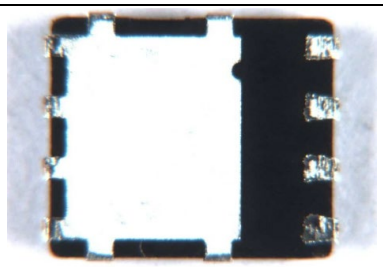
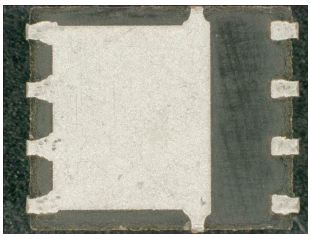
Marking and traceability

The product code marking is the same between plant A and B. Traceability of the BE plant will be ensured by an internal codification (Finished Good) and by the trace code (printed on device top side and on the carton box label). The first two digits of the trace code indicate the back-end plant origin.

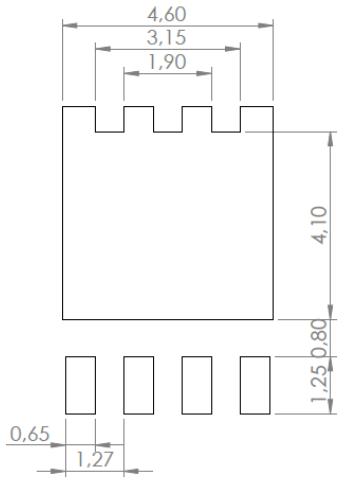
Commercial part number/Order code	Current Finished Good/Type	New Finished Good/Type	Product code marking
STTH30R02DJF-TR	STTH30R02DJFR6/7	STTH30R02DJFR/B	TH30 R02
STTH30R02DJF-TR	TH30R02DJFTR$7	TH30R02DJFTR$B	TH30 R02
STTH5R06DJF-TR	STTH5R06DJFR6/7	STTH5R06DJFR/B	TH5R 06
STTH8R03DJF-TR	STTH8R03DJFR6/7	STTH8R03DJFR/B	TH8R 03
STPS15L30CDJFTR	PS15L30CDJFR6%7	PS15L30CDJFRH%B	PS15L 30C
STPS30H100DJF-TR	PS30H100DJFR6%7	PS30H100DJFTR%B	PS30H 100
STPS30L30DJF-TR	PS30L30DJFR6%7	PS30L30DJFTR%B	PS30 L30
STPS30M60DJF-TR	PS30M60DJFR6%7	PS30M60DJFTR%B	PS30 M60

Current Label (Example for other Rectifier product)	New Label (Example for other Rectifier product)
FG ending by 7	FG ending by B
	

	Current (Location A)	New (Location B)
Top view		

Bottom view		

Recommended Footprint (Location A and Location B compatible)

New **(Location A and Location B compatible)**


Qualification completion date	**Week 38-2022**

Forecasted sample availability

Product family	Commercial part Number	Availability date
Rectifier	STTH30R02DJF-TR	8 weeks after request
Rectifier	STTH5R06DJF-TR	8 weeks after request
Rectifier	STTH8R03DJF-TR	8 weeks after request
Rectifier	STPS30H100DJF-TR	8 weeks after request
Rectifier	STPS30L30DJF-TR	8 weeks after request
Rectifier	STPS30M60DJF-TR	8 weeks after request

For sample(s) request, please inform FSE (Field Sales Engineer) to insert corresponding **Non-Standard Samples Order** (a single Commercial Product for each request) with **PCN reference** as additional information.

Change implementation schedule

Sales-types	Estimated production start	Estimated first shipments
STTH30R02DJF-TR **STTH5R06DJF-TR** **STTH8R03DJF-TR** **STPS30H100DJF-TR** **STPS30L30DJF-TR** **STPS30M60DJF-TR**	**Week 39-2022**	**Week 47-2022**

Comments:	

Customer's feedback

Please contact your local ST sales representative or quality contact for requests concerning this change notification.
Absence of acknowledgement of this PCN within 30 days of receipt will constitute acceptance of the change
Absence of additional response within 90 days of receipt of this PCN will constitute acceptance of the change

Qualification program and results	19015QRP rev.3 Attached

Reliability Evaluation Report
Qualification of PowerFLAT™ 6x5
at Subcontractor in China

General Information	
Product Line	*Rectifiers*
Product Description	Field Effect, Power Schottky and Ultrafast Rectifiers
Product perimeter	*FERD15S50DFJ-TR, FERD20U50DJF-TR FERD30M100DJF-TR, STPS3045DJF-TR STPS30M100DJF-TR, STPS30120DJF-TR STPS30170DJF-TR, STPS15L30CDJFTR, STPS30H100DJF-TR, STPS30L30DJF-TR, STPS30M60DJF-TR, STTH30R02DJF-TR STTH5R06DJF-TR, STTH8R03DJF-TR*
Product Group	*ADG*
Product division	*Discrete and Filter Division*
Package	*PowerFLAT™ 5x6*
Maturity level step	*Qualified*

Locations	
Wafer fab	*ST CATANIA – ITALY* *ST SINGAPORE*
Assembly plant	*SUBCONTRACTOR –CHINA (998G)*
Reliability Lab	*ST TOURS - FRANCE*
Reliability assessment	Pass

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comments
1.0	04-Dec-2018	7	Isabelle BALLON	Julien MICHELON	FERDxxx qualification: FERD15S50DFJ-TR / FERD20U50DJF-TR FERD30M100DJF-TR
2.0	29-Jan-2019				Power Schottky qualification: STPS3045DJF-TR / STPS30M100DJF-TR STPS30120DJF-TR / STPS30170DJF-TR
3.0	07-Sept-2022	7	Christophe GOIN	Julien Michelon Digitally signed by Julien Michelon Date: 2022.09.07 10:52:05 +02'00'	Additional Power Schottky and Ultrafast rectifiers qualification: STPS30H100DJF-TR STPS30L30DJF-TR / STPS30M60DJF-TR STPS15L30CDJFTR / STTH30R02DJF-TR STTH5R06DJF-TR / STTH8R03DJF-TR

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD 47	Stress-Test-Driven Qualification of Integrated Circuits
JESD 94	Application specific qualification using knowledge based test methodology
JESD 22	Reliability test methods for packaged devices

2 GLOSSARY

SS	Sample Size
HTRB	High Temperature Reverse Bias
THB	Temperature Humidity Bias
TC	Temperature Cycling
UHAST	Unbiased Highly Accelerated Stress Test
RSH	Resistance to Soldering Heat
SD	Solderability
DBT	Dead Bug Test
GD	Generic Data
PC	Pre-conditioning (before test)

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

The objective of this report is to qualify PowerFLAT™ 5x6 at subcontractor in China (998G).

The involved products are listed in table here below:

Commercial Product
FERD15S50DFJ-TR
FERD20U50DJF-TR
FERD30M100DJF-TR
STPS3045DJF-TR
STPS30M100DJF-TR
STPS30120DJF-TR
STPS30170DJF-TR
STPS15L30CDJFTR
STPS30H100DJF-TR
STPS30L30DJF-TR
STPS30M60DJF-TR
STTH30R02DJF-TR
STTH5R06DJF-TR
STTH8R03DJF-TR

The reliability test methodology used follows the JESD47-H: « Stress Test Driven Qualification Methodology ».
The following reliability tests ensuing are:

- TC to ensure the mechanical robustness of the products.
- HTRB to evaluate the risk of contamination from the resin and the assembly process versus the die layout sensitivity.
- THB, UHAST to check the robustness to corrosion and the good package hermeticity.
- RSH, Solderability and DBT to check compatibility of package with customer assembly.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Refer to products datasheets.

4.2 Construction Note

	FERD15S50DJF / FERD20U50DJF / FERD30SM100DJF
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania (ITALY)
Technology / Process family	Field Effect Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST SINGAPORE
Assembly information	
Assembly site	Subcontractor in CHINA *(998G)*
Package description	PowerFLAT™ 5x6
Molding compound	ECOPACK®2 compliant component
Lead finishing/bump solder material	Pure Tin
Final testing information	
Testing location	Subcontractor in CHINA *(998G)*

	STPS3045DJF-TR / STPS30M100DJF-TR / STPS30120DJF-TR / STPS30170DJF-TR STPS15L30CDJFTR / STPS30H100DJF-TR / STPS30L30DJF-TR / STPS30M60DJF-TR
Wafer/Die fab. information	
Wafer fab manufacturing location	ST SINGAPORE
Technology / Process family	Power Schottky
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST SINGAPORE
Assembly information	
Assembly site	Subcontractor in CHINA *(998G)*
Package description	PowerFLAT™ 5x6
Molding compound	ECOPACK®2 compliant component
Lead finishing/bump solder material	Pure Tin
Final testing information	
Testing location	Subcontractor in CHINA *(998G)*

	STTH30R02DJF-TR / STTH5R06DJF-TR / STTH8R03DJF-TR
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Tours (FRANCE)
Technology / Process family	Ultrafast
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Tours (FRANCE)
Assembly information	
Assembly site	Subcontractor in CHINA *(998G)*
Package description	PowerFLAT™ 5x6
Molding compound	ECOPACK®2 compliant component
Lead finishing/bump solder material	Pure Tin
Final testing information	
Testing location	Subcontractor in CHINA *(998G)*

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot #	Commercial Product	Package	Comments
Lot 1	FERD20U50DJF-TR	PowerFLAT™ 5x6	Qualification lots (FERD)
Lot 2	FERD30SM100DJF-TR		
Lot 3			
Lot 4	FERD15S50DJF-TR		
Lot 5	STPS30170DJF-TR	PowerFLAT™ 5x6	Qualification lot (Power Schottky)
Lot 6	STTH8R03DJF-TR	PowerFLAT™ 5x6	Qualification lots (Ultrafast)
Lot 7	STTH5R06DJF-TR	PowerFLAT™ 5x6	

Detailed results in below chapter will refer to these references.

5.2 Test plan and results summary

Test	Std ref.	Conditions	Steps / Duration	SS	Failure/SS						
					L1	L2	L3	L4	L5	L6	L7
Die Oriented Tests											
HTRB	MIL-STD-750-1 M1038-Method A	VR = 80V (0.8*VRRM) Tj=110°C (max avoiding thermal runaway)	1Khrs	287		0/77	0/56		0/77		0/77
Package Oriented Tests											
TC	JESD 22A-104	-65/+150°C 2cy/h	500cy	461	0/77	0/77		0/77	0/76	0/77	0/77
THB	JESD22 A-101	85°C; 85% RH VR=80V (0.8*VRRM)	1Khrs	231		0/77			0/77		0/77
UHAST	JESD22 A-118	130°C 85% RH	96hrs	231		0/77			0/77		0/77
RSH	JESD22 B-111 (SMD)	THS 85%RH / 85°C 168hrs Sn/Pb dipping 260°C	-	60	0/30 (Generic data)					0/30	
SD	JESD22 B-102	Wet ageing SnPb bath 220°C	-	10	0/10 (Generic data)						
		Wet ageing SnAgCu bath 245°C	-	10	0/10 (Generic data)						
		Dry ageing SnPb bath 220°C	-	10	0/10 (Generic data)						
		Dryt ageing SnAgCu bath 245°C	-	10	0/10 (Generic data)						
DBT	DM00112629 (ST internal)	IR reflow after flux deposition	-	30	0/30						

Note: Package-oriented tests (except RSH, SD and DBT) are submitted to preconditioning (PC) before test.

6 ANNEXES

6.1 Tests description

Test name	Description	Purpose
Die Oriented		
HTRB High Temperature Reverse Bias	The diode is biased in static reverse mode at targeted junction temperature.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
UHAST Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
RSH Resistance to Solder Heat	Package is dipped by the leads in a solder bath after initial wet ageing (for SMDs only). Assessment by electrical test + no external crack	To simulate wave soldering process and verify that package will not be thermally damaged during this step.
SD Solderability	Ageing + dipping in a solder bath. Assessment by visual inspection of the leads.	To ensure good wettability of the leads
DBT Dead Bug Test	Leads are covered with soldering flux and are submitted to IR reflow. Assessment by visual inspection of the leads	To ensure good wettability of the leads

Reliability Evaluation Report
Qualification of PowerFLAT™ 6x5
at Subcontractor in China

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Product Group	*ADG*
Product division	*Discrete and Filter Division*
Package	*PowerFLAT™ 5x6*
Maturity level step	*Qualified*

Locations	
Wafer fab	*ST CATANIA – ITALY* *ST SINGAPORE*
Assembly plant	*SUBCONTRACTOR –CHINA (998G)*
Reliability Lab	*ST TOURS - FRANCE*
Reliability assessment	Pass

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Version	Date	Pages	Prepared by	Approved by	Comments
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STPS30170DJF-TR
STPS15L30CDJFTR
STPS30H100DJF-TR
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The reliability test methodology used follows the JESD47-H: « Stress Test Driven Qualification Methodology ».
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Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the robustness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Refer to products datasheets.

4.2 Construction Note

	FERD15S50DJF / FERD20U50DJF / FERD30SM100DJF
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Catania (ITALY)
Technology / Process family	Field Effect Rectifier
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST SINGAPORE
Assembly information	
Assembly site	Subcontractor in CHINA *(998G)*
Package description	PowerFLAT™ 5x6
Molding compound	ECOPACK®2 compliant component
Lead finishing/bump solder material	Pure Tin
Final testing information	
Testing location	Subcontractor in CHINA *(998G)*

	STPS3045DJF-TR / STPS30M100DJF-TR / STPS30120DJF-TR / STPS30170DJF-TR STPS15L30CDJFTR / STPS30H100DJF-TR / STPS30L30DJF-TR / STPS30M60DJF-TR
Wafer/Die fab. information	
Wafer fab manufacturing location	ST SINGAPORE
Technology / Process family	Power Schottky
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST SINGAPORE
Assembly information	
Assembly site	Subcontractor in CHINA *(998G)*
Package description	PowerFLAT™ 5x6
Molding compound	ECOPACK®2 compliant component
Lead finishing/bump solder material	Pure Tin
Final testing information	
Testing location	Subcontractor in CHINA *(998G)*

	STTH30R02DJF-TR / STTH5R06DJF-TR / STTH8R03DJF-TR
Wafer/Die fab. information	
Wafer fab manufacturing location	ST Tours (FRANCE)
Technology / Process family	Ultrafast
Wafer Testing (EWS) information	
Electrical testing manufacturing location	ST Tours (FRANCE)
Assembly information	
Assembly site	Subcontractor in CHINA *(998G)*
Package description	PowerFLAT™ 5x6
Molding compound	ECOPACK®2 compliant component
Lead finishing/bump solder material	Pure Tin
Final testing information	
Testing location	Subcontractor in CHINA *(998G)*

5 TESTS RESULTS SUMMARY

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THB	JESD22 A-101	85°C; 85% RH VR=80V (0.8*VRRM)	1Khrs	231		0/77			0/77		0/77
UHAST	JESD22 A-118	130°C 85% RH	96hrs	231		0/77			0/77		0/77
RSH	JESD22 B-111 (SMD)	THS 85%RH / 85°C 168hrs Sn/Pb dipping 260°C	-	60	0/30 (Generic data)					0/30	
SD	JESD22 B-102	Wet ageing SnPb bath 220°C	-	10	0/10 (Generic data)						
		Wet ageing SnAgCu bath 245°C	-	10	0/10 (Generic data)						
		Dry ageing SnPb bath 220°C	-	10	0/10 (Generic data)						
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DBT	DM00112629 (ST internal)	IR reflow after flux deposition	-	30	0/30						

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THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
UHAST Unbiased Highly Accelerated Stress Test	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
RSH Resistance to Solder Heat	Package is dipped by the leads in a solder bath after initial wet ageing (for SMDs only). Assessment by electrical test + no external crack	To simulate wave soldering process and verify that package will not be thermally damaged during this step.
SD Solderability	Ageing + dipping in a solder bath. Assessment by visual inspection of the leads.	To ensure good wettability of the leads
DBT Dead Bug Test	Leads are covered with soldering flux and are submitted to IR reflow. Assessment by visual inspection of the leads	To ensure good wettability of the leads